|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Number of Slice Registers | 20,783 | 184,304 | 11% |  |
| Number used as Flip Flops | 20,477 |  |  |  |
| Number used as Latches | 306 |  |  |  |
| Number used as Latch-thrus | 0 |  |  |  |
| Number used as AND/OR logics | 0 |  |  |  |
| Number of Slice LUTs | 21,188 | 92,152 | 22% |  |
| Number used as logic | 19,718 | 92,152 | 21% |  |
| Number using O6 output only | 14,259 |  |  |  |
| Number using O5 output only | 286 |  |  |  |
| Number using O5 and O6 | 5,173 |  |  |  |
| Number used as ROM | 0 |  |  |  |
| Number used as Memory | 512 | 21,680 | 2% |  |
| Number used as Dual Port RAM | 376 |  |  |  |
| Number using O6 output only | 0 |  |  |  |
| Number using O5 output only | 48 |  |  |  |
| Number using O5 and O6 | 328 |  |  |  |
| Number used as Single Port RAM | 0 |  |  |  |
| Number used as Shift Register | 136 |  |  |  |
| Number using O6 output only | 136 |  |  |  |
| Number using O5 output only | 0 |  |  |  |
| Number using O5 and O6 | 0 |  |  |  |
| Number used exclusively as route-thrus | 958 |  |  |  |
| Number with same-slice register load | 909 |  |  |  |
| Number with same-slice carry load | 47 |  |  |  |
| Number with other load | 2 |  |  |  |
| Number of occupied Slices | 10,141 | 23,038 | 44% |  |
| Nummber of MUXCYs used | 3,964 | 46,076 | 8% |  |
| Number of LUT Flip Flop pairs used | 28,815 |  |  |  |
| Number with an unused Flip Flop | 9,962 | 28,815 | 34% |  |
| Number with an unused LUT | 7,627 | 28,815 | 26% |  |
| Number of fully used LUT-FF pairs | 11,226 | 28,815 | 38% |  |
| Number of unique control sets | 2,132 |  |  |  |
| Number of slice register sites lost         to control set restrictions | 10,089 | 184,304 | 5% |  |
| Number of bonded [IOBs](M://1/Hdl/GitHead/SynFpga/Hl3GNFPGA/fpga/Hl3IoMain_map.xrpt?&DataKey=IOBProperties) | 246 | 540 | 45% |  |
| Number of LOCed IOBs | 221 | 246 | 89% |  |
| IOB Flip Flops | 90 |  |  |  |
| Number of RAMB16BWERs | 52 | 268 | 19% |  |
| Number of RAMB8BWERs | 25 | 536 | 4% |  |
| Number of BUFIO2/BUFIO2\_2CLKs | 0 | 32 | 0% |  |
| Number of BUFIO2FB/BUFIO2FB\_2CLKs | 0 | 32 | 0% |  |
| Number of BUFG/BUFGMUXs | 16 | 16 | 100% |  |
| Number used as BUFGs | 16 |  |  |  |
| Number used as BUFGMUX | 0 |  |  |  |
| Number of DCM/DCM\_CLKGENs | 1 | 12 | 8% |  |
| Number used as DCMs | 1 |  |  |  |
| Number used as DCM\_CLKGENs | 0 |  |  |  |
| Number of ILOGIC2/ISERDES2s | 0 | 586 | 0% |  |
| Number of IODELAY2/IODRP2/IODRP2\_MCBs | 0 | 586 | 0% |  |
| Number of OLOGIC2/OSERDES2s | 90 | 586 | 15% |  |
| Number used as OLOGIC2s | 90 |  |  |  |
| Number used as OSERDES2s | 0 |  |  |  |
| Number of BSCANs | 2 | 4 | 50% |  |
| Number of BUFHs | 0 | 384 | 0% |  |
| Number of BUFPLLs | 0 | 8 | 0% |  |
| Number of BUFPLL\_MCBs | 0 | 4 | 0% |  |
| Number of DSP48A1s | 4 | 180 | 2% |  |
| Number of GTPA1\_DUALs | 0 | 4 | 0% |  |
| Number of ICAPs | 0 | 1 | 0% |  |
| Number of MCBs | 0 | 4 | 0% |  |
| Number of PCIE\_A1s | 0 | 1 | 0% |  |
| Number of PCILOGICSEs | 0 | 2 | 0% |  |
| Number of PLL\_ADVs | 1 | 6 | 16% |  |
| Number of PMVs | 0 | 1 | 0% |  |
| Number of STARTUPs | 0 | 1 | 0% |  |
| Number of SUSPEND\_SYNCs | 0 | 1 | 0% |  |
| Number of RPM macros | 17 |  |  |  |
| Average Fanout of Non-Clock Nets | 3.55 |  |  |  |